AMENDMENTS TO THE SPECIFICATION

Please amend the fourth and fifth paragraphs on page 5 of the Specification according to the following replacement paragraphs:

Fig. 4 is a side elevational view of the core substrate assembly of Fig. 3 after a [first] dielectric layer has been disposed over the patterned upper metal layer and the prefabricated, integrated electronic component and after [a second] another dielectric layer has been disposed over the patterned lower metal layer;

Fig. 5 is a side elevational view of the core substrate assembly of Fig. 4 after a first metal layer has been laminated on the [first] dielectric layer disposed over the patterned upper metal layer and the prefabricated, integrated electronic component and a second metal layer has been laminated on the [second] dielectric layer disposed over the patterned lower metal layer;

Please amend the third and fourth paragraphs on page 6 of the Specification according to the following replacement paragraphs:

Fig. 12 is a side elevational view of the core substrate assembly of Fig. 2 after a cavity has been placed in the exposed upper surface; ~~and~~

Fig. 13 is a side elevational view of the core substrate assembly of Fig. 12 after a prefabricated, integrated circuit component has been disposed in the cavity; and

Please amend the Specification by adding the following paragraph after the fourth paragraph on page 6 of the Specification:

Fig. 14 is a side elevational view of the core substrate assembly of Fig. 12 after two, prefabricated, integrated circuit components have been disposed in the cavity.

Please amend the third paragraph on page 7 of the Specification according to the following replacement paragraph:

After the metal layers **14** and **16** have been appropriately patterned to expose substrate surfaces **12a** and **12b** (as shown in Fig. 2), a prefabricated integrated circuit component **20** may be coupled to substrate surface **12a** as shown in Fig. 3, or to both substrate surfaces **12a** and **12b** as shown in Fig. 11. In another embodiment of the present invention one or both of the substrate surfaces **12a** and **12b** may have a cavity, generally illustrated as **24** in Fig. 12. The cavity **24** may be formed by any suitable means, such as by milling, cutting or drilling. The prefabricated,

integrated circuit component 20 (e.g., resistors, capacitors, inductors, etc.) may be conveniently disposed in the cavity 24, as shown in Fig. 13. Alternatively, two prefabricated integrated circuit components may be disposed in the cavity. As shown in FIG. 14, cavity 24 accommodates a first integrated circuit component 20' having pads 26' and a second integrated circuit component 20'' having pads 26''.

Please amend the first paragraph on page 9 of the Specification according to the following replacement paragraph:

After the desired number of vias have been formed in the circuit board assembly of Fig. 5, metal layers 40 and 42 are patterned as desired. Subsequently, dielectric layers 60 and 64 are respectively disposed over patterned metal layers 40 and 42 and over vias 46 and 50, as best shown in Fig. 8. (Note: Optionally the material for dielectric layers 60 and 64 may form the filler materials 54b and 58b.) A pair of openings 70 is then formed (e.g., such as by laser drilling or the like) through dielectric layer 60, and at least partly through dielectric layer 30 to expose pads 26 of the integrated circuit component 20. Openings 70 are then metal-lined with a suitable metal (e.g. copper) 72 into electrical contact with pads 26. Such metal-lining may be accomplished by any conventional process, such as by sputtering or by the combination of e-less and electrolytic plating. In addition to openings 70, a plurality of additional openings 76 and 80 may be respectively formed through respective dielectric layers 60 and 64, down to residual metal layers(s) remaining from patterned metal layers 40 and 42, respectively. Openings 76 and 80 are then metal-lined by any conventional process to respectively dispose metal liners 78 and 82 in openings 76 and 80. Subsequently metal layers 94 and 98 may be disposed in dielectric layers 60 and 64 and patterned, such that residual metal layers 94 and 98 are respectively coupled to residual metal layers 40 and 42, respectively, by and through metal liners 78 and 82. Additionally, the circuit board assembly can provide contact between pads 26 and layer 40 through the use of additional conductive layers on the dielectric layers, as is well know in the art. For example, FIG. 9 shows a connection between pad 26' and layer 40'. Pad 26' is in electrical contact with liner 72' and layer 40' is in electrical contact with liner 78', as described above. A conductive layer 95 on dielectric layer 60 connects liners 72' and 78', thereby providing electrical connection between pad 26' and layer 40'. The printed circuit board assembly in Fig. 9 comprises an integrated-electronic-component embedded laminated board which is available for

dielectric build-up by means well known to those skilled in the art (e.g., post plating for stacked via build-up structures).